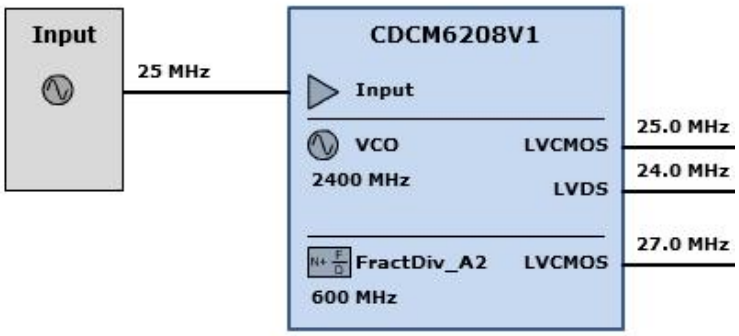
WEBENCH® Clock Architect

Project Report

Project: 4066381/39 Project 39 - [CDCM6208V1]
Created: 8/12/16 8:36:45 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

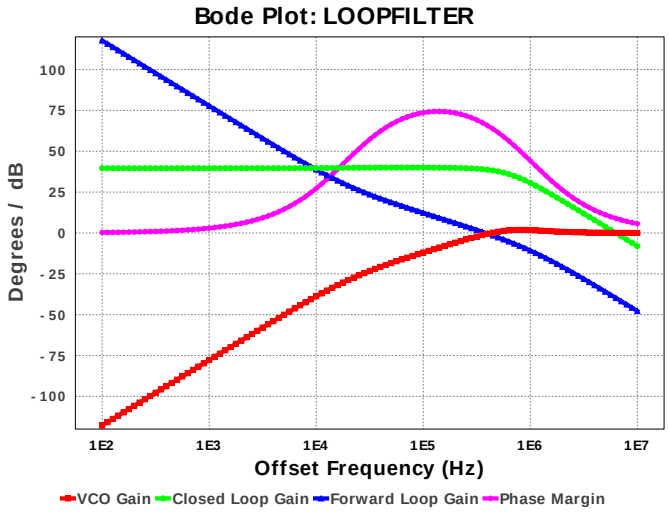
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	137.5 mA
Total Footprint	49.0 mm^2

User ID = 4066381
Design Id = 234
Device = CDCM6208V1
Created = 8/12/16 8:36:45 AM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V1 LOOPFILTER



Preferences

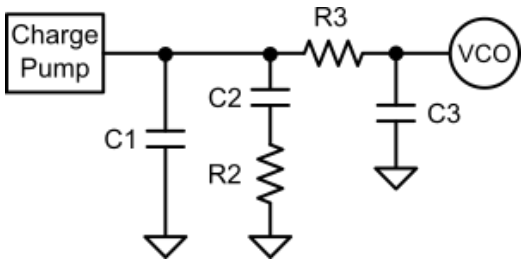
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	382.1136767405222 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	24
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	423.625 kHz	N	382.114 kHz
Phase Margin	65.00 deg	N	66.447 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	7.626

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	0.56 kohms	N	N
R3	0.10 kohms	Y	N



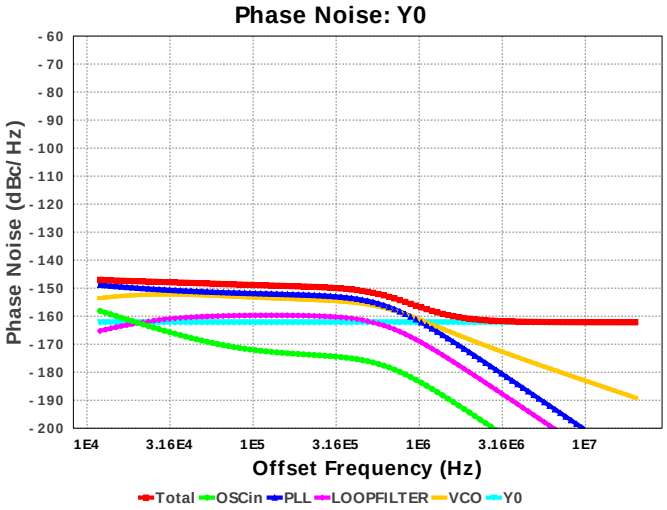
Output Block: CDCM6208V1 CDCM6208V1 : Y0 as LVDS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-160.038 dBc/Hz
RMS Jitter	417.439 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.063 mrad
EVM	0.006%
SNR	84.02 dB
Spur	-87.02 dBc
Jitter (Pk-Pk)	2976.546 fs
Jitter (Cycle to Cycle Pk)	5953.092 fs
Jitter (Cycle to Cycle RMS)	590.348 fs
A/D ENOB	13.671 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	Y0
12 kHz	-146.99	-158.11	-148.82	-165.25	-153.52	-162.2
100 kHz	-148.87	-172.02	-151.81	-159.74	-153.32	-162.2
20000 kHz	-162.19	-234.09	-212.61	-219.7	-189.09	-162.2



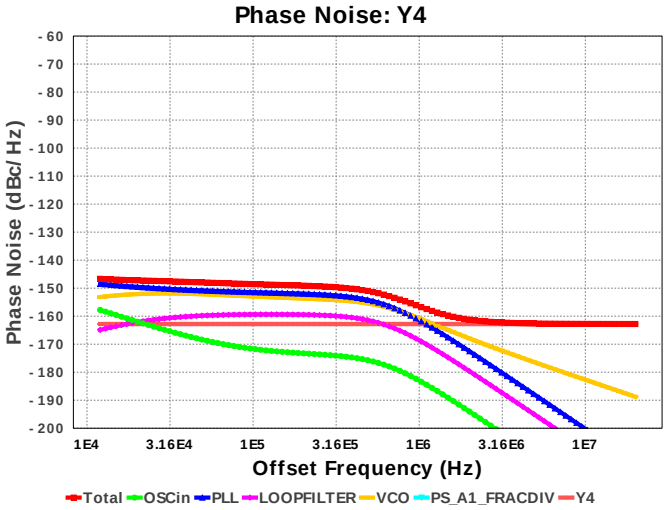
Output Block: CDCM6208V1 CDCM6208V1 : Y4 as LVCMOS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-160.239 dBc/Hz
RMS Jitter	391.603 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.062 mrad
EVM	0.006%
SNR	84.221 dB
Spur	-87.221 dBc
Jitter (Pk-Pk)	2792.326 fs
Jitter (Cycle to Cycle Pk)	5584.652 fs
Jitter (Cycle to Cycle RMS)	553.811 fs
A/D ENOB	13.704 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A1_FRACDIV	Y4
12 kHz	-146.66	-157.76	-148.47	-164.9	-153.17	-1000	-162.8
100 kHz	-148.55	-171.67	-151.46	-159.38	-152.96	-1000	-162.8
20000 kHz	-162.79	-233.74	-212.26	-219.35	-188.74	-1000	-162.8



Output Block: CDCM6208V1 CDCM6208V1 : Y5 as LVCMOS output, 26+23301686/23301689 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.499 dBc/Hz
RMS Jitter	883.868 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.15 mrad
EVM	0.015%
SNR	76.481 dB
Spur	-79.481 dBc
Jitter (Pk-Pk)	6302.418 fs
Jitter (Cycle to Cycle Pk)	12604.836 fs
Jitter (Cycle to Cycle RMS)	1249.978 fs
A/D ENOB	12.419 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A2_FRACDIV	Y5
12 kHz	-145.27	-157.09	-147.8	-164.23	-152.5	-153.37	-162.8
100 kHz	-146.82	-171	-150.79	-158.72	-152.29	-153.37	-162.8
20000 kHz	-152.9	-233.07	-211.59	-218.68	-188.07	-153.37	-162.8