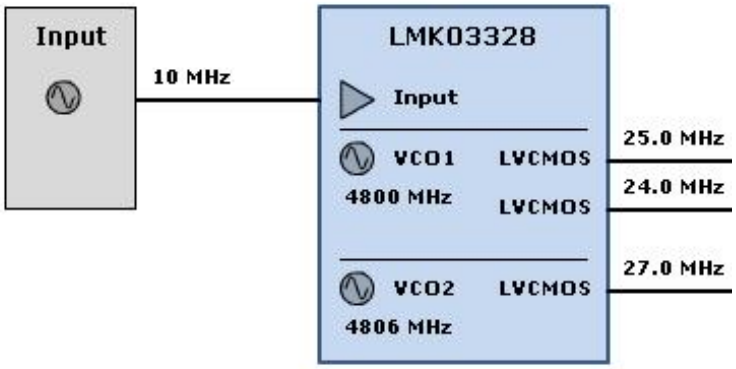
WEBENCH® Clock Architect

Project Report

Project: 3473280/4 Project 4 - [LMK03328]
Created: 8/2/16 4:37:26 PM



Block Diagram

My Comments
LMK03328

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No

Properties

Name	Design Value
External Sources	none
Total BOM Cost	$10.0
Total Current	402.5 mA
Total Footprint	49.0 mm^2

User ID = 3473280
Design Id = 64
Device = LMK03328
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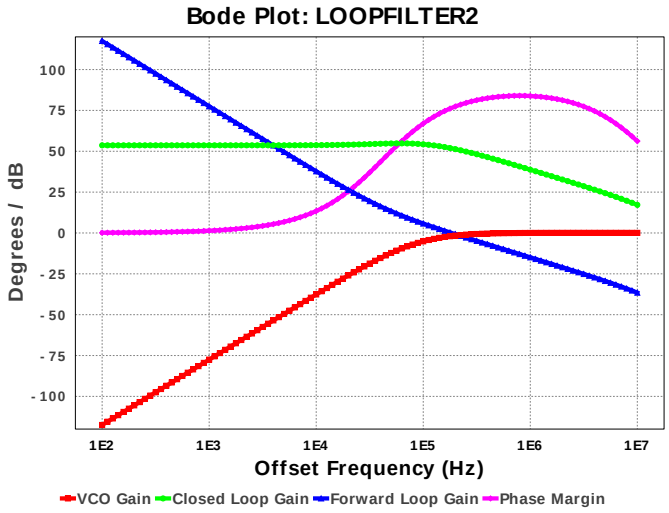
WEBENCH® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



Preferences

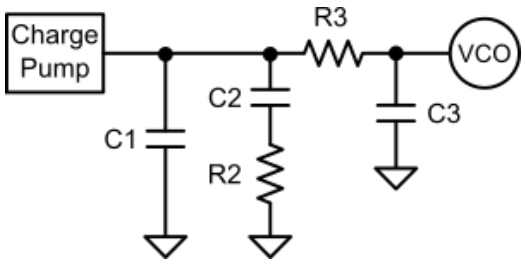
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	45.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4806.00 MHz
Phase Det. Frequency	10.00 MHz
Filter type	designed
Brickwall Bandwidth	183.97436209108182 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	480
PLL Numerator	3.0
PLL Denominator	5.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

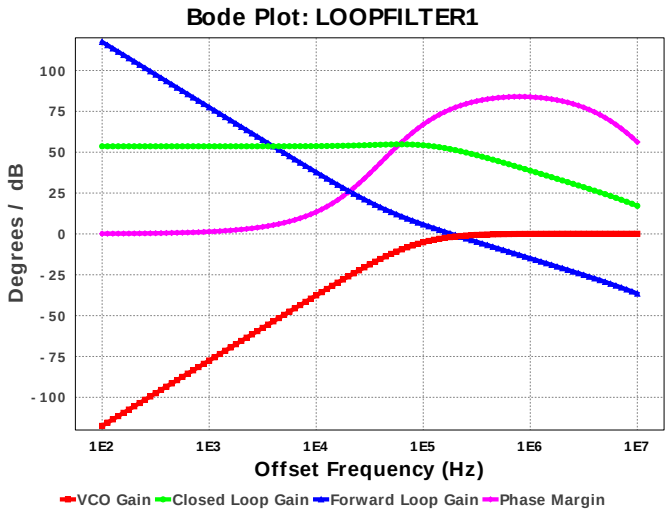
Name	Design Value	Forced	Actual Value
Loop Bandwidth	138.919 kHz	N	183.974 kHz
Phase Margin	70.00 deg	N	76.51 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.054

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	1.80 nF	N	N
C3	Open	Y	N
C4	Open	N	N
R2	2.117 kohms	Y	N
R3	6.299 kohms	Y	N



Loop Filter: LMK03328 LOOPFILTER1



Preferences

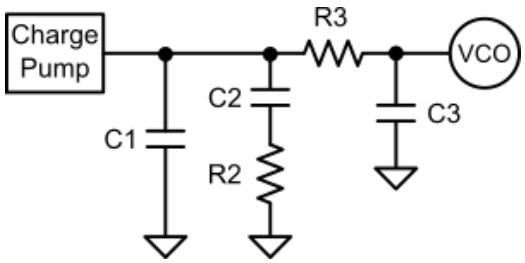
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	45.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4800.00 MHz
Phase Det. Frequency	10.00 MHz
Filter type	designed
Brickwall Bandwidth	183.75572181658458 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	480
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	138.919 kHz	N	183.756 kHz
Phase Margin	70.00 deg	N	76.496 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.054

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	1.80 nF	N	N
C3	Open	Y	N
C4	Open	N	N
R2	2.117 kohms	Y	N
R3	6.299 kohms	Y	N



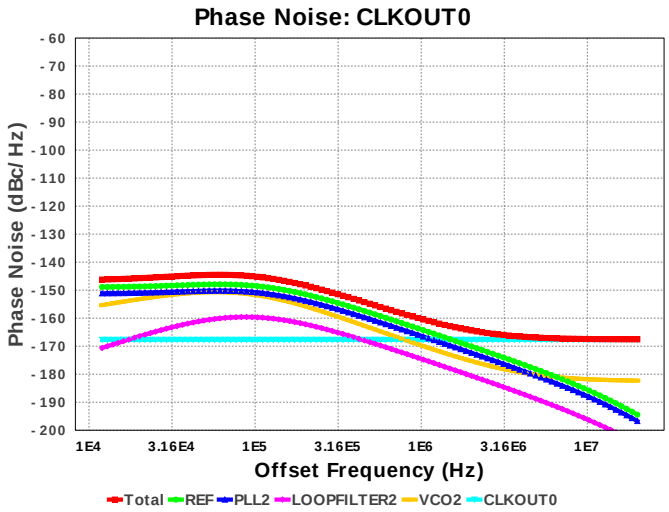
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVCMOS output, 27.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.222 dBc/Hz
RMS Jitter	288.57 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.049 mrad
EVM	0.005%
SNR	86.204 dB
Spur	-89.204 dBc
Jitter (Pk-Pk)	2057.645 fs
Jitter (Cycle to Cycle Pk)	4115.289 fs
Jitter (Cycle to Cycle RMS)	408.099 fs
A/D ENOB	14.034 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL2	LOOPFILTER2	VCO2	CLKOUT0
12 kHz	-146.22	-148.86	-151.14	-170.62	-155.33	-167.71
100 kHz	-145.14	-148.47	-150.75	-159.66	-151.7	-167.71
20000 kHz	-167.55	-194.43	-196.72	-204.39	-182.28	-167.71



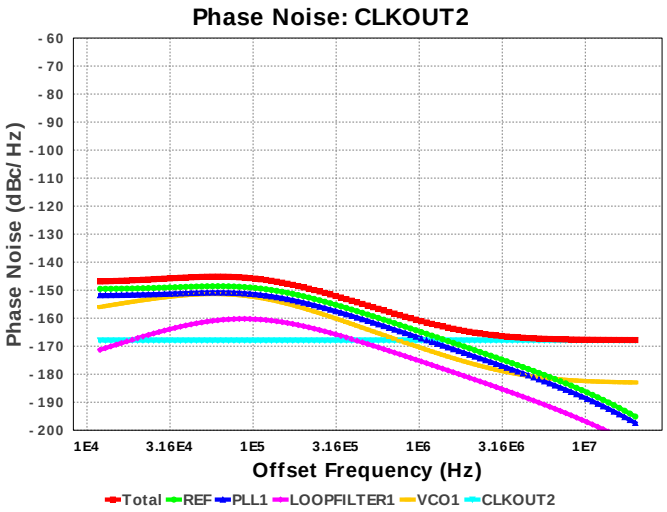
Output Block: LMK03328 LMK03328 : CLKOUT2 as LVCMOS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.765 dBc/Hz
RMS Jitter	292.756 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.046 mrad
EVM	0.005%
SNR	86.747 dB
Spur	-89.747 dBc
Jitter (Pk-Pk)	2087.493 fs
Jitter (Cycle to Cycle Pk)	4174.986 fs
Jitter (Cycle to Cycle RMS)	414.019 fs
A/D ENOB	14.124 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL1	LOOPFILTER1	VCO1	CLKOUT2
12 kHz	-146.88	-149.53	-151.8	-171.29	-155.99	-167.95
100 kHz	-145.8	-149.14	-151.42	-160.33	-152.37	-167.95
20000 kHz	-167.8	-195.11	-197.4	-205.07	-182.94	-167.95



Output Block: LMK03328 LMK03328 : CLKOUT4 as LVCMOS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-163.08 dBc/Hz
RMS Jitter	294.122 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.044 mrad
EVM	0.004%
SNR	87.062 dB
Spur	-90.062 dBc
Jitter (Pk-Pk)	2097.238 fs
Jitter (Cycle to Cycle Pk)	4194.476 fs
Jitter (Cycle to Cycle RMS)	415.952 fs
A/D ENOB	14.176 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL1	LOOPFILTER1	VCO1	CLKOUT4
12 kHz	-147.24	-149.88	-152.16	-171.65	-156.35	-168.17
100 kHz	-146.16	-149.49	-151.77	-160.68	-152.73	-168.17
20000 kHz	-168.02	-195.46	-197.75	-205.43	-183.3	-168.17