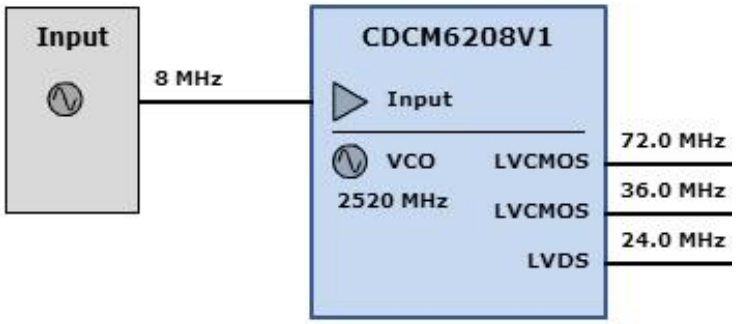
WEBENCH® Clock Architect

Project Report

Project: 4412135/2 Project 2 - [CDCM6208V1]
Created: 8/1/16 7:57:21 PM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	32	Any	1
fixed2	72	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No

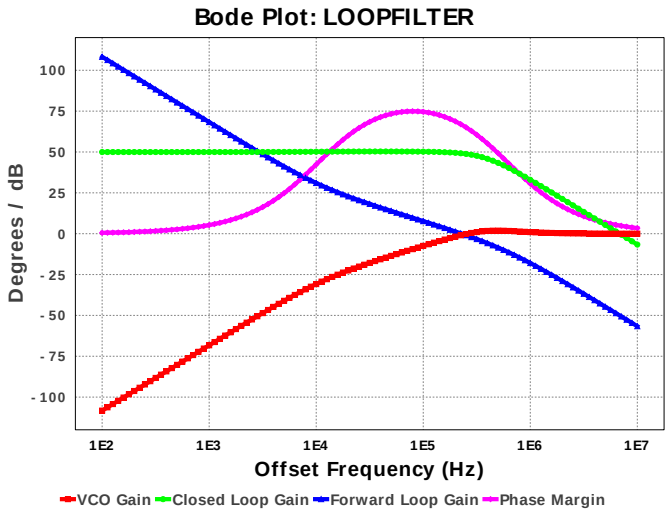
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	132.5 mA
Total Footprint	49.0 mm^2

User ID = 4412135
Design Id = 8
Device = CDCM6208V1
Created = 8/1/16 7:57:21 PM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V1 LOOPFILTER



Preferences

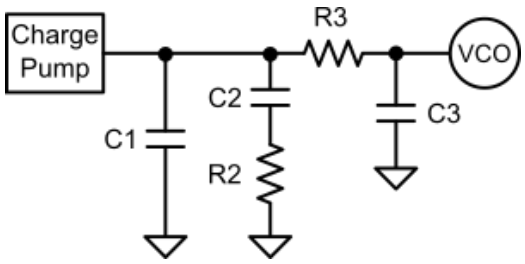
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2520.00 MHz
Phase Det. Frequency	8.00 MHz
Filter type	designed
Brickwall Bandwidth	228.4647213509527 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	63
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	258.091 kHz	N	228.465 kHz
Phase Margin	65.00 deg	N	66.693 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	8.114

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	1.00 kohms	N	N
R3	0.10 kohms	Y	N



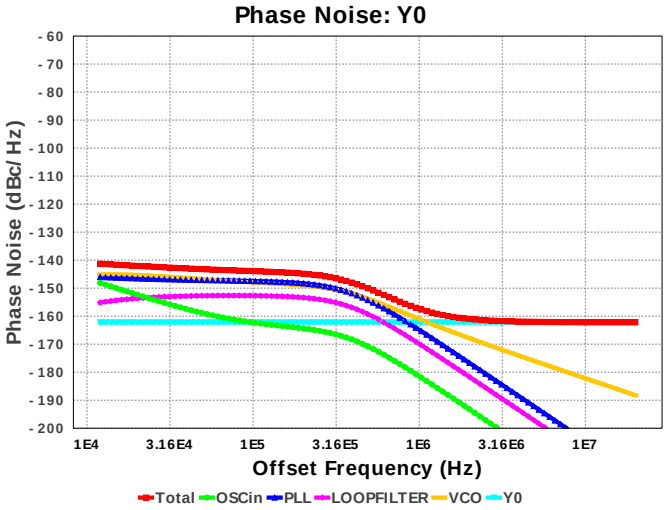
Output Block: CDCM6208V1 CDCM6208V1 : Y0 as LVDS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-158.489 dBc/Hz
RMS Jitter	498.934 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.075 mrad
EVM	0.008%
SNR	82.471 dB
Spur	-85.471 dBc
Jitter (Pk-Pk)	3557.646 fs
Jitter (Cycle to Cycle Pk)	7115.293 fs
Jitter (Cycle to Cycle RMS)	705.599 fs
A/D ENOB	13.414 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	Y0
12 kHz	-141.27	-148.12	-146.03	-155.15	-145.14	-162.2
100 kHz	-143.91	-162.26	-147.47	-152.69	-147.92	-162.2
20000 kHz	-162.19	-233.1	-216.57	-221.53	-188.21	-162.2



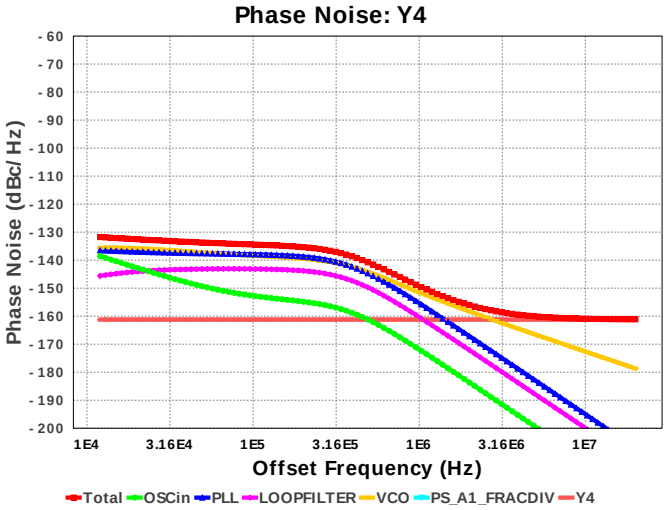
Output Block: CDCM6208V1 CDCM6208V1 : Y4 as LVCMOS output, 72.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-150.927 dBc/Hz
RMS Jitter	397.211 fs
RMS Phase Error (deg)	0.01 deg
RMS Phase Error	0.18 mrad
EVM	0.018%
SNR	74.909 dB
Spur	-77.909 dBc
Jitter (Pk-Pk)	2832.311 fs
Jitter (Cycle to Cycle Pk)	5664.622 fs
Jitter (Cycle to Cycle RMS)	561.741 fs
A/D ENOB	12.158 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A1_FRACDIV	Y4
12 kHz	-131.76	-138.58	-136.49	-145.61	-135.6	-1000	-161.21
100 kHz	-134.42	-152.72	-137.93	-143.15	-138.37	-1000	-161.21
20000 kHz	-161.14	-223.56	-207.03	-211.99	-178.67	-1000	-161.21



Output Block: CDCM6208V1 CDCM6208V1 : Y5 as LVCMOS output, 36.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.28 dBc/Hz
RMS Jitter	428.964 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.097 mrad
EVM	0.01%
SNR	80.262 dB
Spur	-83.262 dBc
Jitter (Pk-Pk)	3058.728 fs
Jitter (Cycle to Cycle Pk)	6117.456 fs
Jitter (Cycle to Cycle RMS)	606.647 fs
A/D ENOB	13.047 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A2_FRACDIV	Y5
12 kHz	-137.77	-144.6	-142.51	-151.63	-141.62	-1000	-162.8
100 kHz	-140.43	-158.74	-143.95	-149.17	-144.39	-1000	-162.8
20000 kHz	-162.77	-229.58	-213.05	-218.01	-184.69	-1000	-162.8