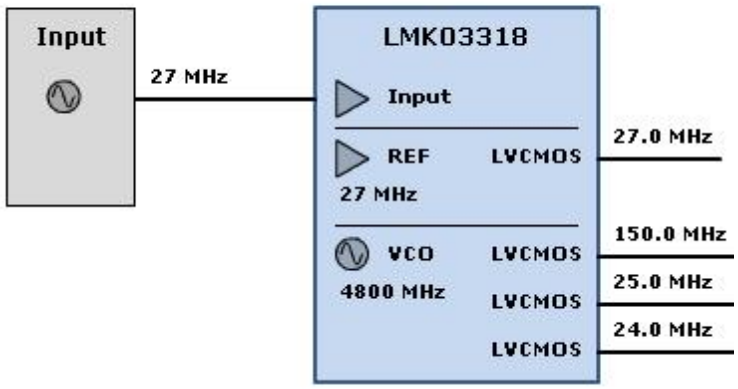
WEBENCH® Clock Architect

Project Report

Project: 1194016/452 Project 452 - [LMK03318]
Created: 7/25/16 7:35:33 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1
fixed_0	150	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

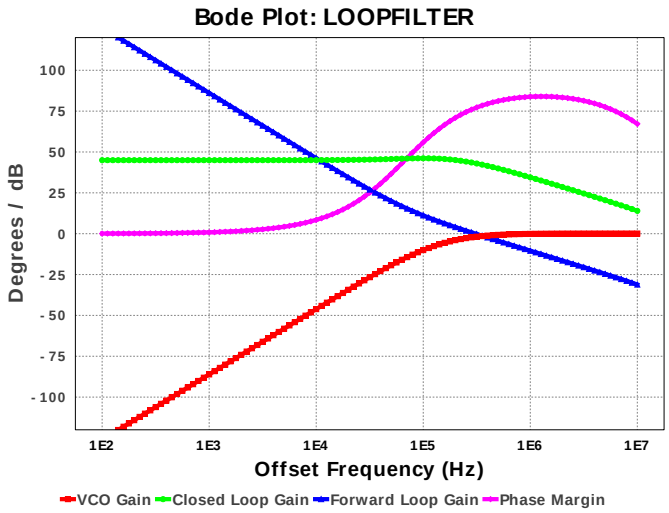
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$7.5
Total Current	320.0 mA
Total Footprint	49.0 mm^2

User ID = 1194016
Design Id = 2226
Device = LMK03318
Created = 7/25/16 7:35:33 AM

WEBENCH ® Clock Design Report

Loop Filter: LMK03318 LOOPFILTER



Preferences

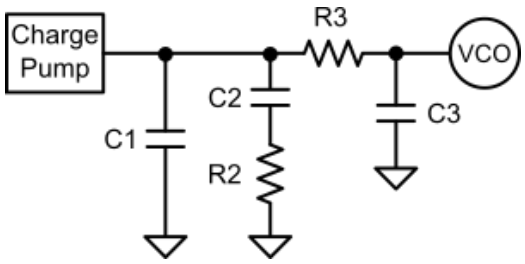
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	45.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4800.00 MHz
Phase Det. Frequency	27.00 MHz
Filter type	designed
Brickwall Bandwidth	308.0392425793467 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	177
PLL Numerator	7.0
PLL Denominator	9.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	228.019 kHz	N	308.039 kHz
Phase Margin	70.00 deg	N	76.977 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.058

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	1.80 nF	N	N
C3	Open	Y	N
C4	Open	N	N
R2	1.317 kohms	Y	N
R3	6.299 kohms	Y	N



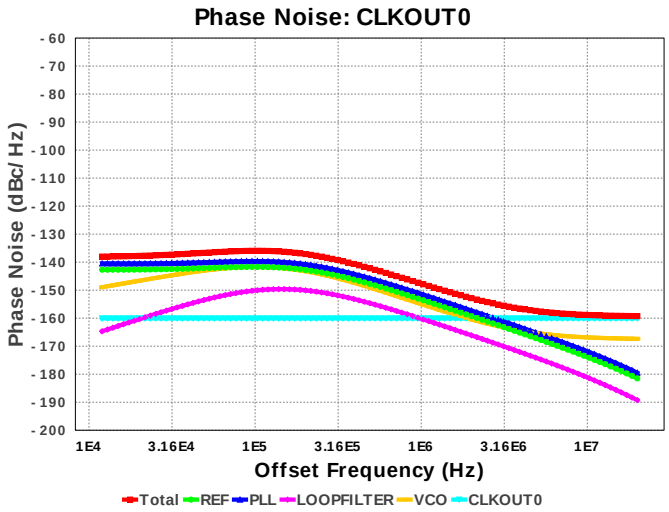
Output Block: LMK03318 LMK03318 : CLKOUT0 as LVCMOS output, 150.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-151.921 dBc/Hz
RMS Jitter	170.05 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.16 mrad
EVM	0.016%
SNR	75.903 dB
Spur	-78.903 dBc
Jitter (Pk-Pk)	1212.541 fs
Jitter (Cycle to Cycle Pk)	2425.082 fs
Jitter (Cycle to Cycle RMS)	240.487 fs
A/D ENOB	12.323 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-138.02	-142.69	-140.46	-164.67	-148.94	-160.07
100 kHz	-135.94	-141.69	-139.63	-150.11	-141.72	-160.07
20000 kHz	-159.26	-181.49	-179.46	-189.26	-167.35	-160.07



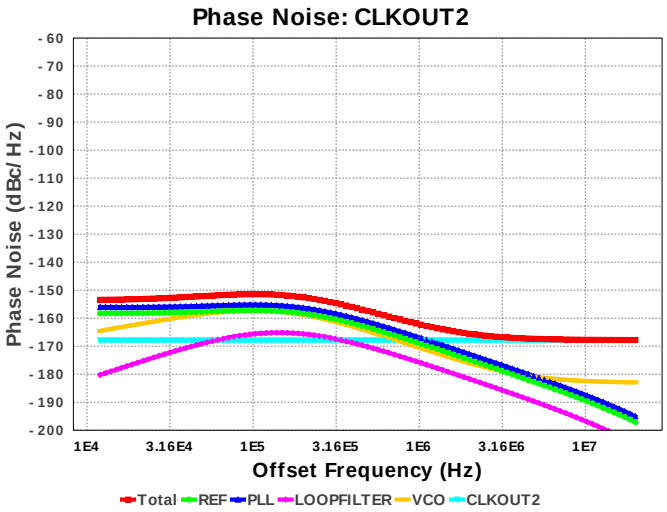
Output Block: LMK03318 LMK03318 : CLKOUT2 as LVCMOS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-165.063 dBc/Hz
RMS Jitter	224.704 fs
RMS Phase Error (deg)	0.002 deg
RMS Phase Error	0.035 mrad
EVM	0.004%
SNR	89.045 dB
Spur	-92.045 dBc
Jitter (Pk-Pk)	1602.249 fs
Jitter (Cycle to Cycle Pk)	3204.499 fs
Jitter (Cycle to Cycle RMS)	317.779 fs
A/D ENOB	14.506 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL	LOOPFILTER	VCO	CLKOUT2
12 kHz	-153.45	-158.25	-156.03	-180.24	-164.51	-167.95
100 kHz	-151.43	-157.26	-155.2	-165.67	-157.29	-167.95
20000 kHz	-167.8	-197.05	-195.03	-204.82	-182.92	-167.95



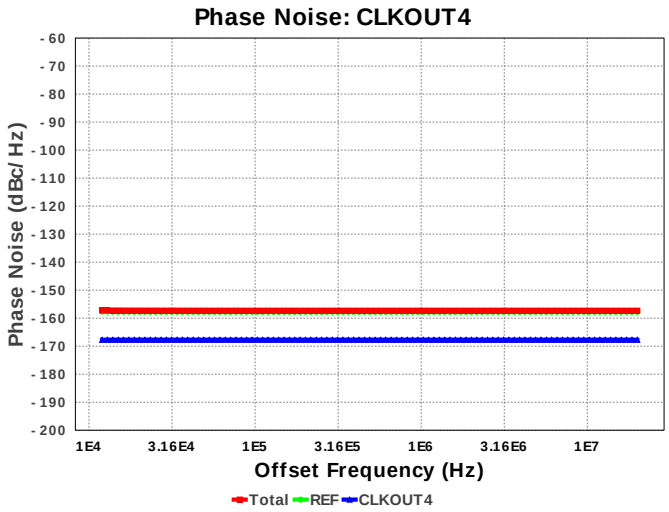
Output Block: LMK03318 LMK03318 : CLKOUT4 as LVCMOS output, 27.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-157.325 dBc/Hz
RMS Jitter	507.111 fs
RMS Phase Error (deg)	0.005 deg
RMS Phase Error	0.086 mrad
EVM	0.009%
SNR	81.307 dB
Spur	-84.307 dBc
Jitter (Pk-Pk)	3615.95 fs
Jitter (Cycle to Cycle Pk)	7231.90 fs
Jitter (Cycle to Cycle RMS)	717.163 fs
A/D ENOB	13.22 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	CLKOUT4
12 kHz	-157.24	-157.64	-167.71
100 kHz	-157.32	-157.74	-167.71
20000 kHz	-157.33	-157.74	-167.71



Output Block: LMK03318 LMK03318 : CLKOUT5 as LVCMOS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-165.35 dBc/Hz
RMS Jitter	226.481 fs
RMS Phase Error (deg)	0.002 deg
RMS Phase Error	0.034 mrad
EVM	0.003%
SNR	89.332 dB
Spur	-92.332 dBc
Jitter (Pk-Pk)	1614.925 fs
Jitter (Cycle to Cycle Pk)	3229.849 fs
Jitter (Cycle to Cycle RMS)	320.293 fs
A/D ENOB	14.553 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	REF	PLL	LOOPFILTER	VCO	CLKOUT5
12 kHz	-153.8	-158.61	-156.38	-180.59	-164.86	-168.17
100 kHz	-151.78	-157.61	-155.55	-166.03	-157.64	-168.17
20000 kHz	-168.02	-197.41	-195.38	-205.18	-183.27	-168.17