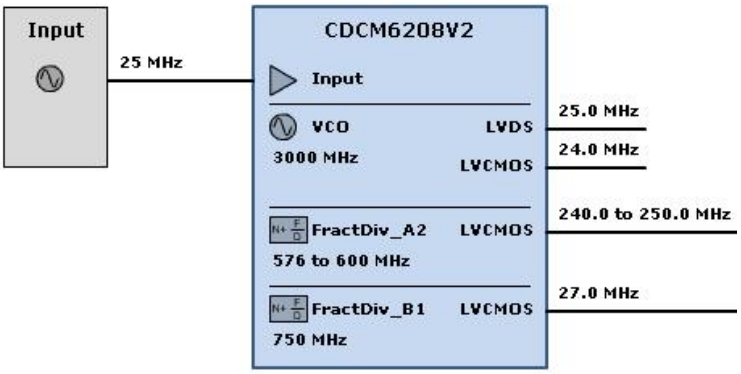
WEBENCH® Clock Architect

Project Report

Project: 1194016/440 Project 440 - [CDCM6208V2]
Created: 7/20/16 5:54:09 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

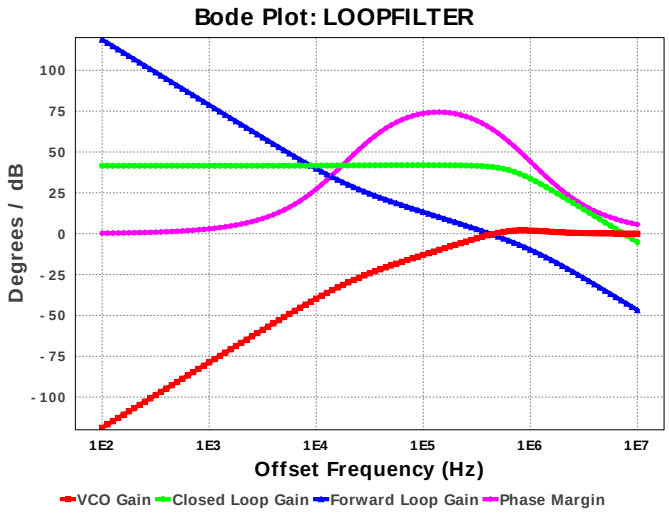
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	157.9 mA
Total Footprint	49.0 mm^2

User ID = 1194016
Design Id = 2132
Device = CDCM6208V2
Created = 7/20/16 5:54:09 AM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V2 LOOPFILTER



Preferences

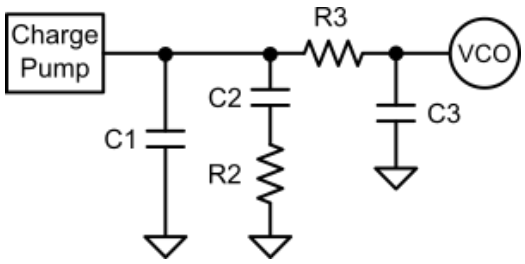
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	250.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	3000.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	421.96398042132466 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	30
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	423.625 kHz	N	421.964 kHz
Phase Margin	65.00 deg	N	64.764 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	9.30

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	0.56 kohms	N	N
R3	0.10 kohms	Y	N



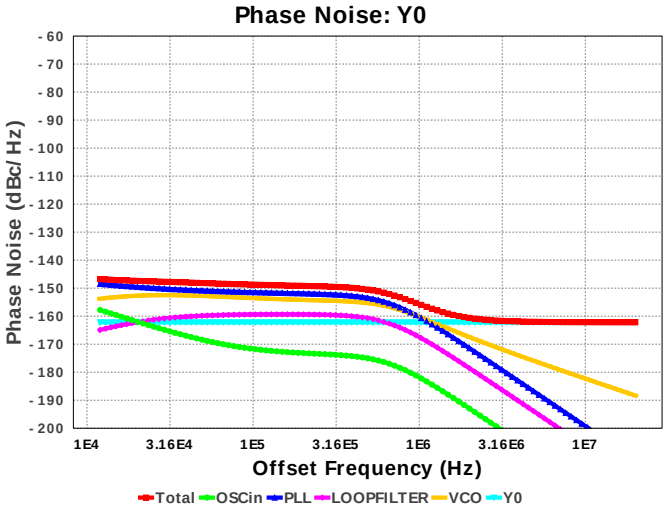
Output Block: CDCM6208V2 CDCM6208V2 : Y0 as LVDS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-159.785 dBc/Hz
RMS Jitter	412.622 fs
RMS Phase Error (deg)	0.004 deg
RMS Phase Error	0.065 mrad
EVM	0.006%
SNR	83.767 dB
Spur	-86.767 dBc
Jitter (Pk-Pk)	2942.202 fs
Jitter (Cycle to Cycle Pk)	5884.403 fs
Jitter (Cycle to Cycle RMS)	583.536 fs
A/D ENOB	13.629 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	Y0
12 kHz	-146.78	-157.77	-148.48	-164.91	-153.75	-162.2
100 kHz	-148.74	-171.68	-151.47	-159.4	-153.55	-162.2
20000 kHz	-162.19	-232.76	-211.27	-218.37	-188.33	-162.2



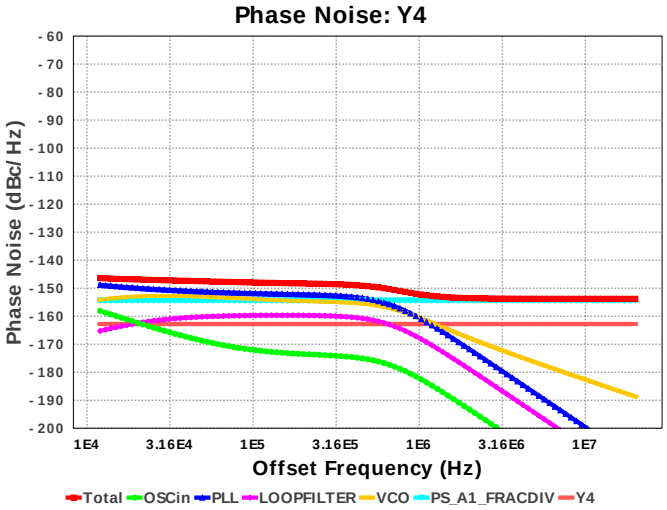
Output Block: CDCM6208V2 CDCM6208V2 : Y4 as LVCMOS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-153.393 dBc/Hz
RMS Jitter	897.158 fs
RMS Phase Error (deg)	0.008 deg
RMS Phase Error	0.135 mrad
EVM	0.014%
SNR	77.375 dB
Spur	-80.375 dBc
Jitter (Pk-Pk)	6397.184 fs
Jitter (Cycle to Cycle Pk)	12794.367 fs
Jitter (Cycle to Cycle RMS)	1268.774 fs
A/D ENOB	12.567 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A1_FRACDIV	Y4
12 kHz	-146.39	-158.13	-148.84	-165.26	-154.11	-154.39	-162.8
100 kHz	-147.98	-172.04	-151.83	-159.75	-153.9	-154.39	-162.8
20000 kHz	-153.8	-233.11	-211.63	-218.72	-188.69	-154.39	-162.8



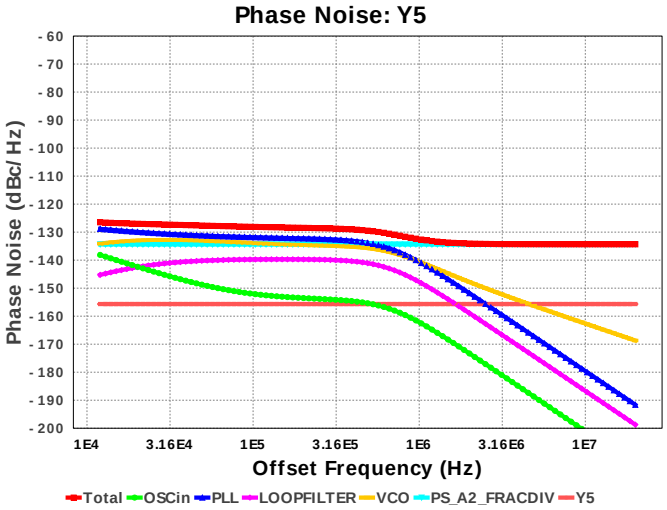
Output Block: CDCM6208V2 CDCM6208V2 : Y5 as LVCMOS output, 240.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-133.893 dBc/Hz
RMS Jitter	846.995 fs
RMS Phase Error (deg)	0.073 deg
RMS Phase Error	1.277 mrad
EVM	0.128%
SNR	57.875 dB
Spur	-60.875 dBc
Jitter (Pk-Pk)	6039.496 fs
Jitter (Cycle to Cycle Pk)	12078.991 fs
Jitter (Cycle to Cycle RMS)	1197.832 fs
A/D ENOB	9.328 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A2_FRACDIV	Y5
12 kHz	-126.49	-138.13	-128.84	-145.26	-134.11	-134.39	-155.67
100 kHz	-128.12	-152.04	-131.83	-139.75	-133.9	-134.39	-155.67
20000 kHz	-134.35	-213.11	-191.63	-198.72	-168.69	-134.39	-155.67



Output Block: CDCM6208V2 CDCM6208V2 : Y6 as LVCMOS output, 26+3640886/3640889 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.475 dBc/Hz
RMS Jitter	886.301 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.15 mrad
EVM	0.015%
SNR	76.458 dB
Spur	-79.458 dBc
Jitter (Pk-Pk)	6319.766 fs
Jitter (Cycle to Cycle Pk)	12639.533 fs
Jitter (Cycle to Cycle RMS)	1253.419 fs
A/D ENOB	12.415 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_B1_FRACDIV	Y6
12 kHz	-145.39	-157.1	-147.81	-164.24	-153.09	-153.37	-162.8
100 kHz	-146.99	-171.01	-150.8	-158.73	-152.88	-153.37	-162.8
20000 kHz	-152.9	-232.09	-210.61	-217.7	-187.66	-153.37	-162.8