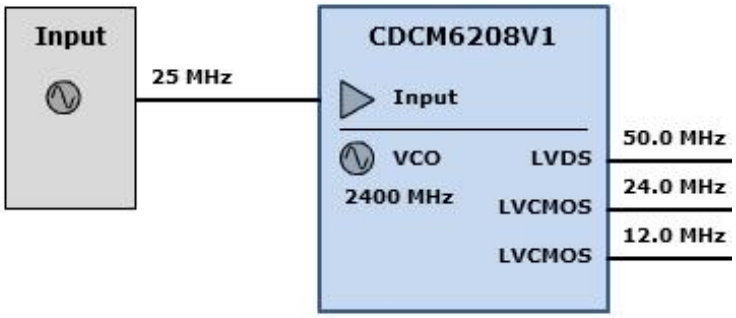
WEBENCH® Clock Architect

Project Report

Project: 1899731/8 Project 8 - [CDCM6208V1]
Created: 7/13/16 4:44:18 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	50	Any	1
fixed1	24	Any	1
fixed2	12	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

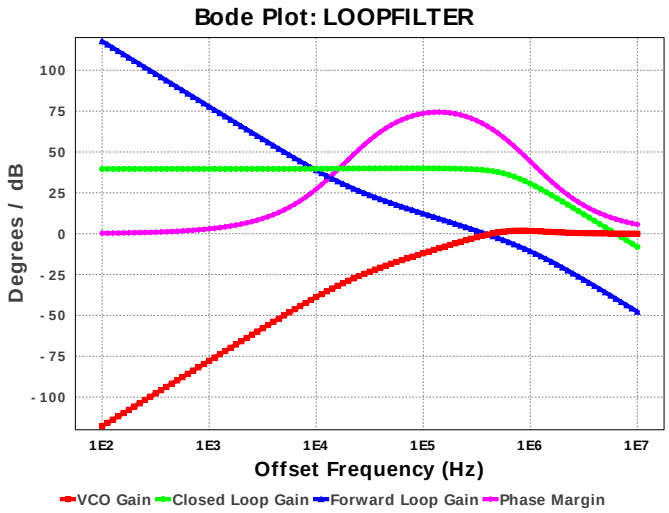
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	132.5 mA
Total Footprint	49.0 mm^2

User ID = 1899731
Design Id = 80
Device = CDCM6208V1
Created = 7/13/16 4:44:18 AM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V1 LOOPFILTER



Preferences

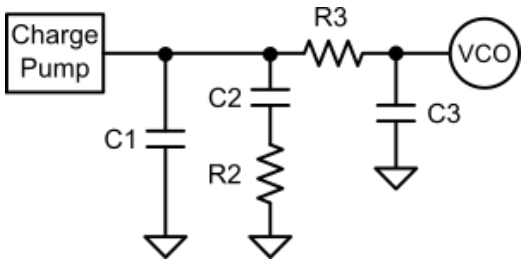
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2400.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	382.1136767405222 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	24
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	423.625 kHz	N	382.114 kHz
Phase Margin	65.00 deg	N	66.447 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	7.626

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	0.56 kohms	N	N
R3	0.10 kohms	Y	N



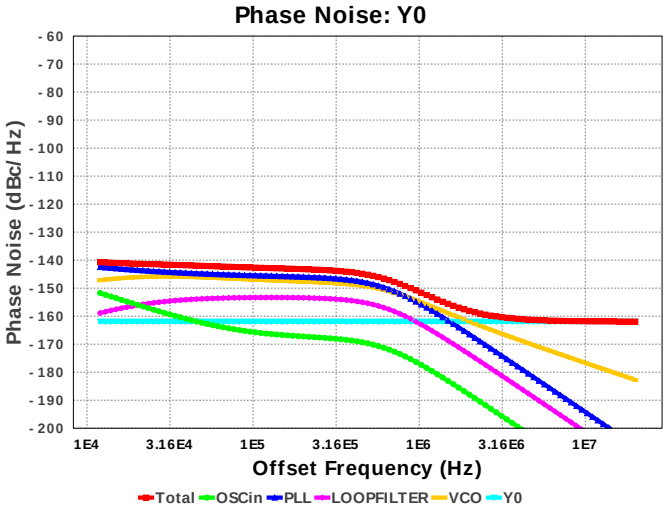
Output Block: CDCM6208V1 CDCM6208V1 : Y0 as LVDS output, 50.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.338 dBc/Hz
RMS Jitter	306.787 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.096 mrad
EVM	0.01%
SNR	80.32 dB
Spur	-83.32 dBc
Jitter (Pk-Pk)	2187.541 fs
Jitter (Cycle to Cycle Pk)	4375.081 fs
Jitter (Cycle to Cycle RMS)	433.862 fs
A/D ENOB	13.057 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	Y0
12 kHz	-140.71	-151.74	-142.45	-158.88	-147.15	-161.96
100 kHz	-142.65	-165.65	-145.44	-153.36	-146.94	-161.96
20000 kHz	-161.92	-227.72	-206.24	-213.33	-182.72	-161.96



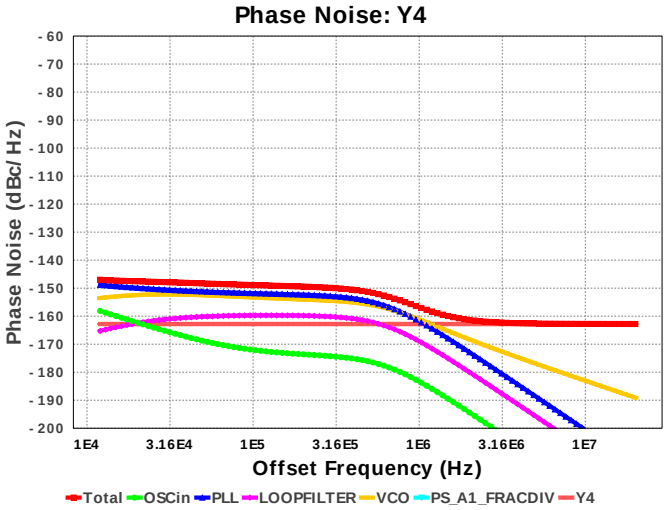
Output Block: CDCM6208V1 CDCM6208V1 : Y4 as LVCMOS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-160.393 dBc/Hz
RMS Jitter	400.732 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.06 mrad
EVM	0.006%
SNR	84.375 dB
Spur	-87.375 dBc
Jitter (Pk-Pk)	2857.421 fs
Jitter (Cycle to Cycle Pk)	5714.841 fs
Jitter (Cycle to Cycle RMS)	566.721 fs
A/D ENOB	13.73 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A1_FRACDIV	Y4
12 kHz	-147.01	-158.11	-148.82	-165.25	-153.52	-1000	-162.8
100 kHz	-148.9	-172.02	-151.81	-159.74	-153.32	-1000	-162.8
20000 kHz	-162.79	-234.09	-212.61	-219.7	-189.09	-1000	-162.8



Output Block: CDCM6208V1 CDCM6208V1 : Y5 as LVCMOS output, 12.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.062 dBc/Hz
RMS Jitter	661.339 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.05 mrad
EVM	0.005%
SNR	86.044 dB
Spur	-89.044 dBc
Jitter (Pk-Pk)	4715.672 fs
Jitter (Cycle to Cycle Pk)	9431.344 fs
Jitter (Cycle to Cycle RMS)	935.274 fs
A/D ENOB	14.007 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	PS_A2_FRACDIV	Y5
12 kHz	-152.7	-164.14	-154.84	-171.27	-159.54	-1000	-162.8
100 kHz	-154.42	-178.04	-157.84	-165.76	-159.34	-1000	-162.8
20000 kHz	-162.8	-240.11	-218.63	-225.73	-195.11	-1000	-162.8