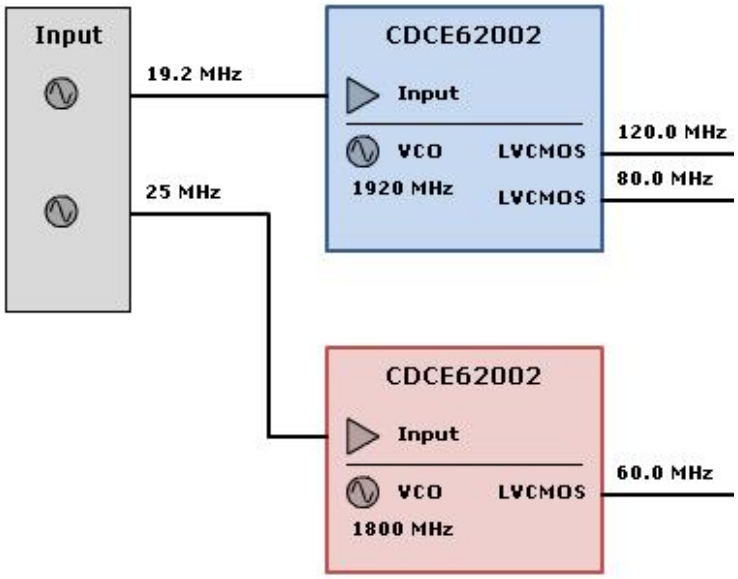
WEBENCH® Clock Architect

Project Report

Project: 1194016/433 Project 433 - [CDCE62002, CDCE62002]
Created: 7/13/16 7:18:07 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	60	Any	1
fixed1	80	Any	1
fixed2	120	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes
Part Filter	CDCE62002

Properties

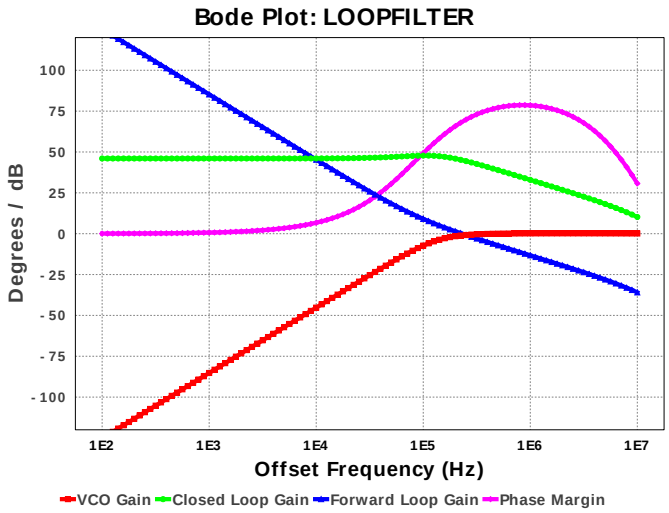
Name	Design Value
External Sources	none
Total BOM Cost	$13.2

Name	Design Value
Total Current	353.5 mA
Total Footprint	50.0 mm^2

User ID = 1194016
Design Id = 2102
Device = CDCE62002
Created = 7/13/16 7:18:07 AM

WEBENCH ® Clock Design Report

Loop Filter: CDCE62002 LOOPFILTER



Preferences

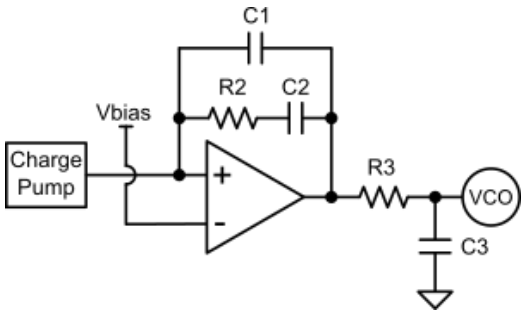
Name	Design Value
Filter Type	Active B
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	1.50 mA
VCO Gain	50.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1920.00 MHz
Phase Det. Frequency	9.60 MHz
Filter type	designed
Brickwall Bandwidth	231.2160918945529 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	100
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	258.091 kHz	N	231.216 kHz
Phase Margin	70.00 deg	N	68.489 deg
T3/T1Ratio	50.00 %	N	208.993 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.074

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.002 nF	Y	N
C2	0.474 nF	Y	N
C3	0.002 nF	Y	N
C4	Open	Y	N
R2	4.00 kohms	Y	N
R3	5.00 kohms	Y	N



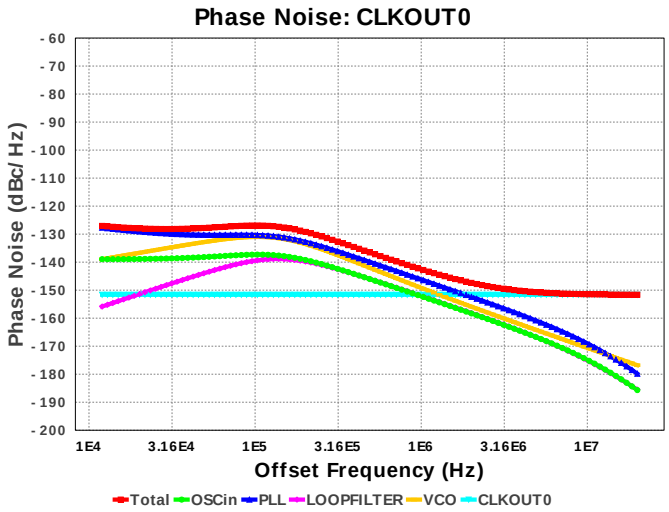
Output Block: CDCE62002 CDCE62002 : CLKOUT0 as LVCMOS output, 120.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-144.508 dBc/Hz
RMS Jitter	499.021 fs
RMS Phase Error (deg)	0.022 deg
RMS Phase Error	0.376 mrad
EVM	0.038%
SNR	68.49 dB
Spur	-71.49 dBc
Jitter (Pk-Pk)	3558.265 fs
Jitter (Cycle to Cycle Pk)	7116.53 fs
Jitter (Cycle to Cycle RMS)	705.722 fs
A/D ENOB	11.091 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-127.07	-138.94	-127.69	-155.85	-138.96	-151.63
100 kHz	-126.92	-137.31	-130.32	-139.48	-130.99	-151.63
20000 kHz	-151.61	-185.66	-179.81	-185.5	-176.78	-151.63



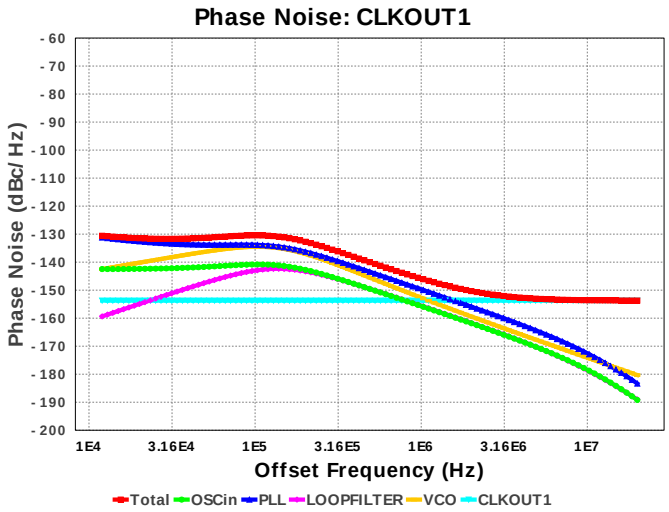
Output Block: CDCE62002 CDCE62002 : CLKOUT1 as LVCMOS output, 80.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-147.713 dBc/Hz
RMS Jitter	517.593 fs
RMS Phase Error (deg)	0.015 deg
RMS Phase Error	0.26 mrad
EVM	0.026%
SNR	71.695 dB
Spur	-74.695 dBc
Jitter (Pk-Pk)	3690.695 fs
Jitter (Cycle to Cycle Pk)	7381.39 fs
Jitter (Cycle to Cycle RMS)	731.987 fs
A/D ENOB	11.624 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT1
12 kHz	-130.58	-142.46	-131.22	-159.37	-142.48	-153.72
100 kHz	-130.44	-140.83	-133.84	-143	-134.51	-153.72
20000 kHz	-153.7	-189.19	-183.34	-189.02	-180.3	-153.72



User ID = 1194016
Design Id = 2103
Device = CDCE62002
Created = 7/13/16 7:18:07 AM

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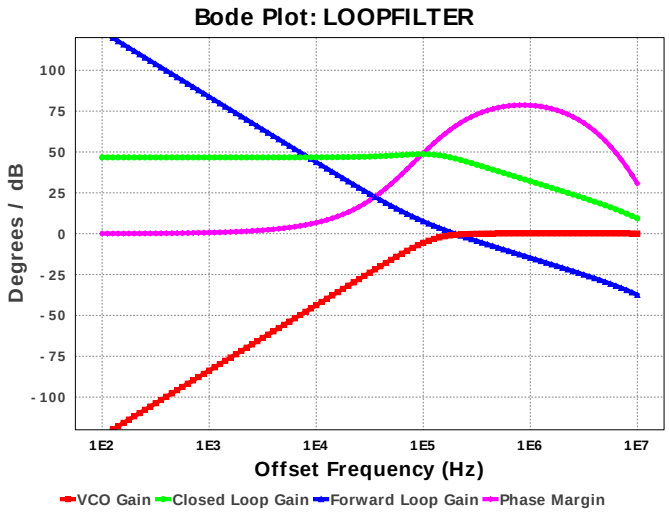
Loop Filter: CDCE62002 LOOPFILTER



Preferences

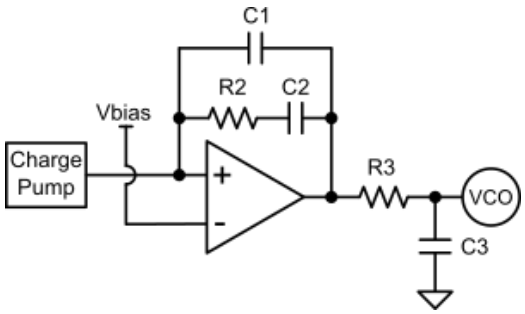
Name	Design Value
Filter Type	Active B
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	1.50 mA
VCO Gain	50.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1800.00 MHz
Phase Det. Frequency	8.333 MHz
Filter type	designed
Brickwall Bandwidth	199.25650706500127 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	72
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	258.091 kHz	N	199.257 kHz
Phase Margin	70.00 deg	N	65.808 deg
T3/T1Ratio	50.00 %	N	208.993 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.055

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.002 nF	Y	N
C2	0.474 nF	Y	N
C3	0.002 nF	Y	N
C4	Open	Y	N
R2	4.00 kohms	Y	N
R3	5.00 kohms	Y	N


C1
R2
C2
Vbias
Charge
Pump
+
-
R3
VCO
C3

Output Block: CDCE62002 CDCE62002 : CLKOUT0 as LVCMOS output, 60.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-149.727 dBc/Hz
RMS Jitter	547.27 fs
RMS Phase Error (deg)	0.012 deg
RMS Phase Error	0.206 mrad
EVM	0.021%
SNR	73.709 dB
Spur	-76.709 dBc
Jitter (Pk-Pk)	3902.304 fs
Jitter (Cycle to Cycle Pk)	7804.608 fs
Jitter (Cycle to Cycle RMS)	773.956 fs
A/D ENOB	11.958 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-132.89	-147.24	-133.52	-160.63	-143.34	-155.24
100 kHz	-131.87	-145.39	-135.63	-144.04	-135.16	-155.24
20000 kHz	-155.23	-195.45	-186.69	-191.76	-182.65	-155.24