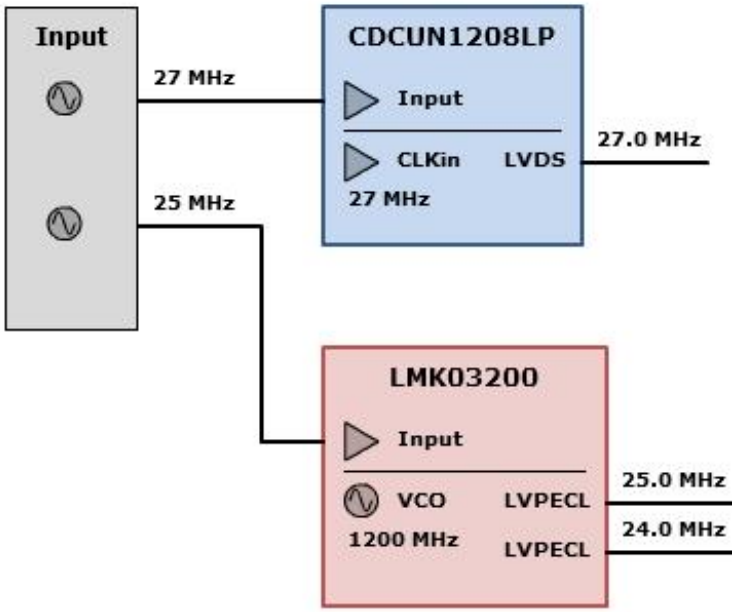
WEBENCH® Clock Architect

Project Report

Project: 4354344/9 Project 9 - [CDCUN1208LP, LMK03200]
Created: 7/13/16 12:32:49 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

Properties

Name	Design Value
External Sources	none
Total BOM Cost	$14.3

Name	Design Value
Total Current	212.5 mA
Total Footprint	74.0 mm^2

User ID = 4354344
Design Id = 38
Device = CDCUN1208LP
Created = 7/13/16 12:32:49 AM

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User ID = 4354344
Design Id = 39
Device = LMK03200
Created = 7/13/16 12:32:49 AM

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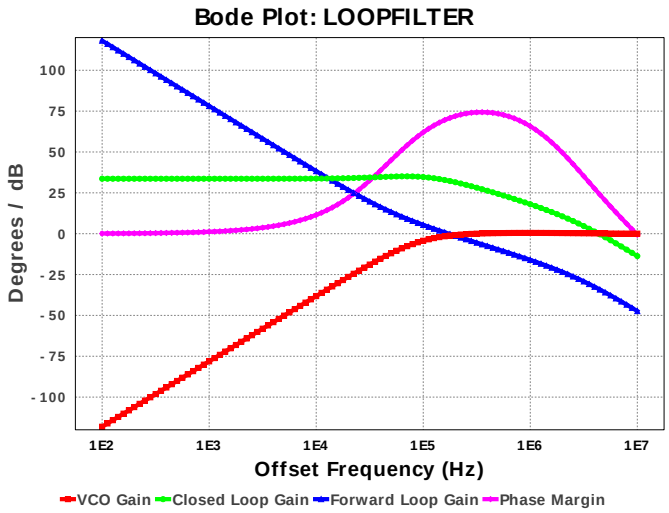
Loop Filter: LMK03200 LOOPFILTER



Preferences

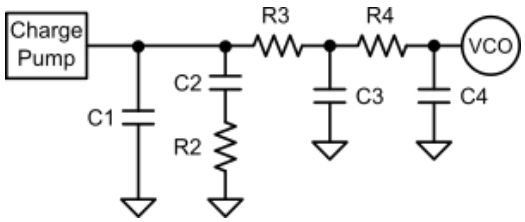
Name	Design Value
Filter Type	Passive
Filter Order	4th Order
Op Amp Gain	1.00
Charge Pump Gain	3.20 mA
VCO Gain	8.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1200.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	172.95451866960593 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	48
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	177.978 kHz	N	172.955 kHz
Phase Margin	70.00 deg	N	70.56 deg
T3/T1Ratio	50.00 %	N	7.845 %
T4/T3Ratio	50.00 %	N	0.00 %
Gamma	0.24	N	0.242

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.015 nF	N	N
C2	1.50 nF	N	N
C3	Open	Y	N
C4	0.01 nF	Y	N
R2	2.20 kohms	N	N
R3	0.60 kohms	Y	N
R4	0.20 kohms	Y	N



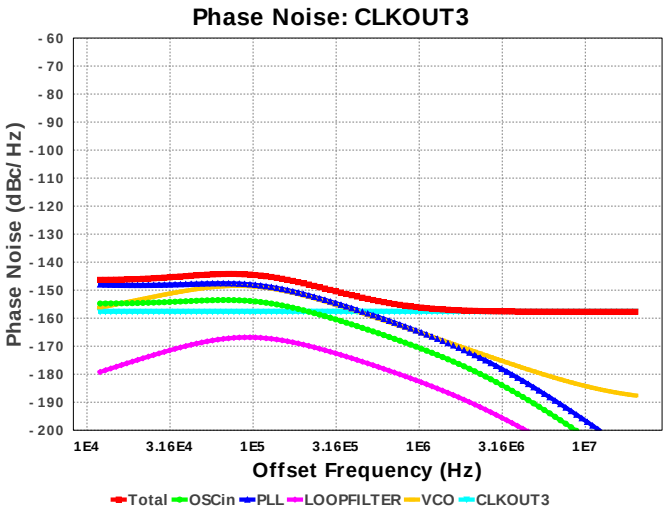
Output Block: LMK03200 LMK03200 : CLKOUT3 as LVPECL output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.712 dBc/Hz
RMS Jitter	587.749 fs
RMS Phase Error (deg)	0.005 deg
RMS Phase Error	0.092 mrad
EVM	0.009%
SNR	80.694 dB
Spur	-83.694 dBc
Jitter (Pk-Pk)	4190.94 fs
Jitter (Cycle to Cycle Pk)	8381.88 fs
Jitter (Cycle to Cycle RMS)	831.202 fs
A/D ENOB	13.119 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT3
12 kHz	-146.32	-154.77	-147.99	-179.21	-156.21	-157.7
100 kHz	-144.53	-153.95	-148.06	-166.88	-148.65	-157.7
20000 kHz	-157.7	-215.04	-209.29	-219.74	-187.6	-157.7



Output Block: LMK03200 LMK03200 : CLKOUT4 as LVPECL output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.785 dBc/Hz
RMS Jitter	607.108 fs
RMS Phase Error (deg)	0.005 deg
RMS Phase Error	0.092 mrad
EVM	0.009%
SNR	80.767 dB
Spur	-83.767 dBc
Jitter (Pk-Pk)	4328.981 fs
Jitter (Cycle to Cycle Pk)	8657.961 fs
Jitter (Cycle to Cycle RMS)	858.58 fs
A/D ENOB	13.131 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT4
12 kHz	-146.65	-155.13	-148.34	-179.56	-156.57	-157.7
100 kHz	-144.87	-154.3	-148.41	-167.23	-149	-157.7
20000 kHz	-157.7	-215.39	-209.65	-220.09	-187.95	-157.7