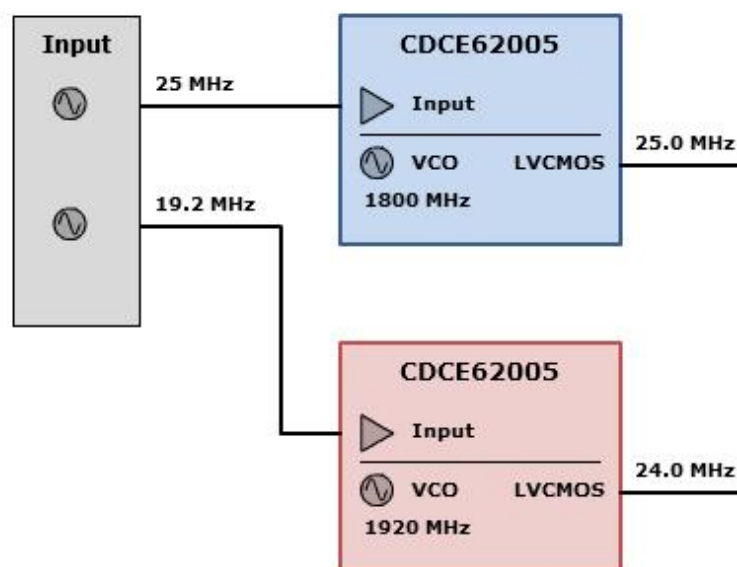


WEBENCH[®] Clock Architect

Project Report

Project: 4354344/10 Project 10 - [CDCE62005, CDCE62005]

Created: 7/13/16 1:37:59 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select	Yes
Input Frequencies	
Part Filter	CDCE62005

Properties

Name	Design Value
External Sources	none
Total BOM Cost	\$15.0
Total Current	517.6 mA

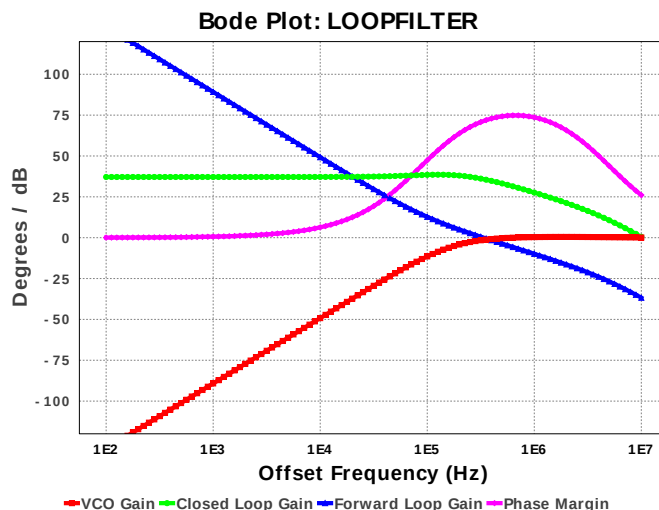
Name	Design Value
Total Footprint	98.0 mm ²



User ID = 4354344
 Design Id = 48
 Device = CDCE62005
 Created = 7/13/16 1:37:59 AM

WEBENCH® Clock Design Report

Loop Filter: CDCE62005 LOOPFILTER



Preferences

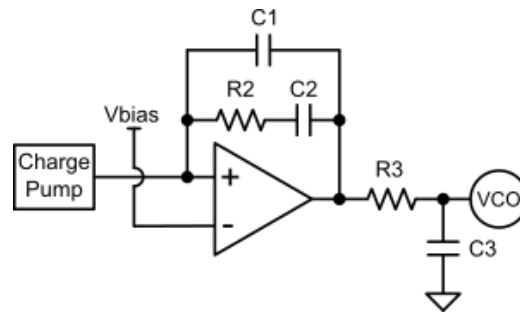
Name	Design Value
Filter Type	Active B
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.00 mA
VCO Gain	50.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1800.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	336.0385040468958 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	36
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	330.657 kHz	N	336.039 kHz
Phase Margin	70.00 deg	N	71.414 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	50.00 %	N	0.00 %
Gamma	0.24	N	0.255

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.018 nF	N	N
C2	1.00 nF	N	N
C3	Open	Y	N
C4	Open	Y	N
R2	1.80 kohms	N	N



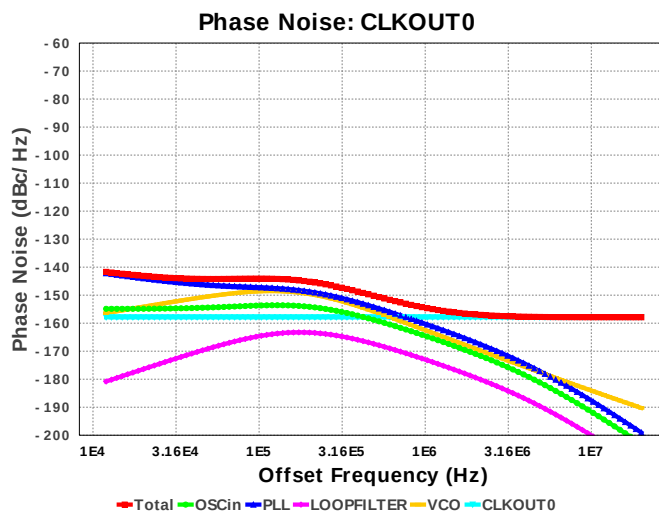
Output Block: CDCE62005 CDCE62005 : CLKOUT0 as LVCMOS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.25 dBc/Hz
RMS Jitter	619.809 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.097 mrad
EVM	0.01%
SNR	80.232 dB
Spur	-83.232 dBc
Jitter (Pk-Pk)	4419.546 fs
Jitter (Cycle to Cycle Pk)	8839.092 fs
Jitter (Cycle to Cycle RMS)	876.543 fs
A/D ENOB	13.042 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-141.69	-154.88	-142.18	-180.81	-156.39	-157.9
100 kHz	-144.09	-153.7	-147.19	-164.64	-148.63	-157.9
20000 kHz	-157.9	-203.03	-199.04	-211.46	-190.25	-157.9

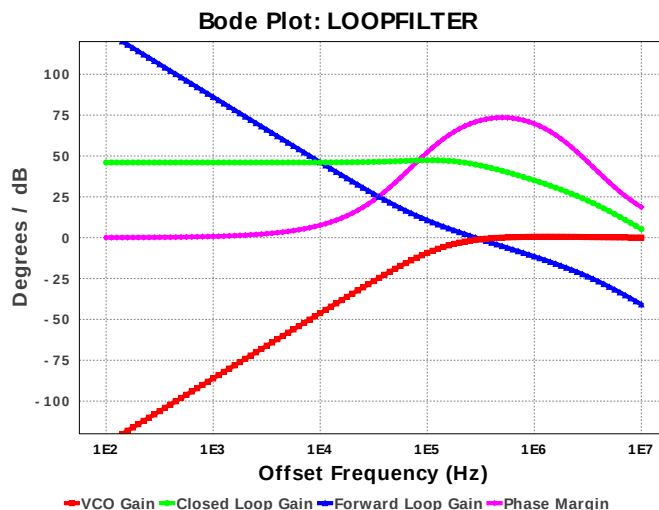




User ID = 4354344
 Design Id = 49
 Device = CDCE62005
 Created = 7/13/16 1:37:59 AM

WEBENCH® Clock Design Report

Loop Filter: CDCE62005 LOOPFILTER



Preferences

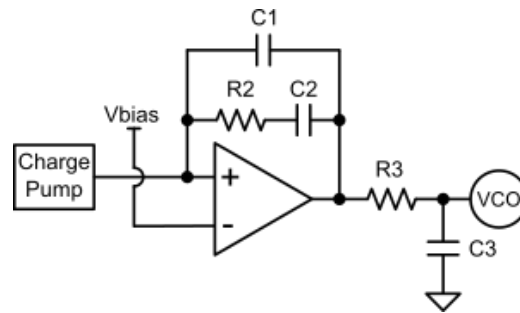
Name	Design Value
Filter Type	Active B
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.00 mA
VCO Gain	50.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	1920.00 MHz
Phase Det. Frequency	9.60 MHz
Filter type	designed
Brickwall Bandwidth	285.4468206974557 kHz
Delta Sigma Order	0
Randomization Factor	0.0 %
PLL Whole Part	100
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	258.091 kHz	N	285.447 kHz
Phase Margin	70.00 deg	N	70.981 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	50.00 %	N	0.00 %
Gamma	0.24	N	0.322

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.012 nF	N	N
C2	0.56 nF	N	N
C3	Open	Y	N
C4	Open	Y	N
R2	3.90 kohms	N	N



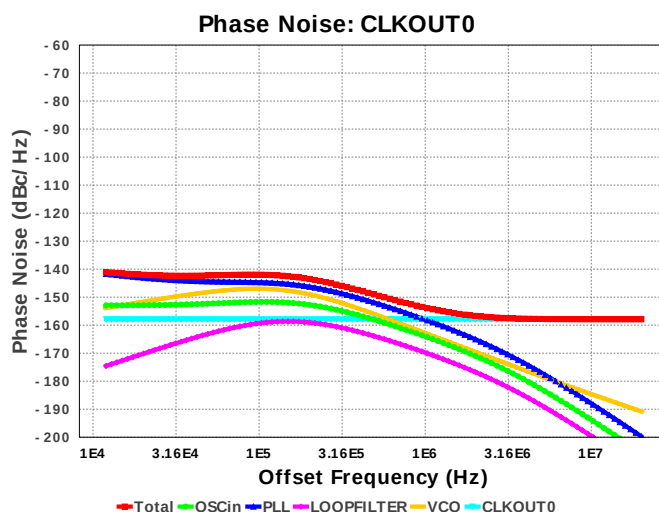
Output Block: CDCE62005 CDCE62005 : CLKOUT0 as LVCMOS output, 24.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-155.663 dBc/Hz
RMS Jitter	690.846 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.104 mrad
EVM	0.01%
SNR	79.645 dB
Spur	-82.645 dBc
Jitter (Pk-Pk)	4926.073 fs
Jitter (Cycle to Cycle Pk)	9852.146 fs
Jitter (Cycle to Cycle RMS)	977.004 fs
A/D ENOB	12.944 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-141.04	-152.92	-141.68	-174.55	-153.86	-157.9
100 kHz	-141.98	-151.69	-144.69	-159.31	-147.02	-157.9
20000 kHz	-157.9	-205.53	-199.68	-211.3	-190.78	-157.9



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